



KOREA UNIVERSITY
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Software Safety and Dependable Systems

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1981~1991

KAIST

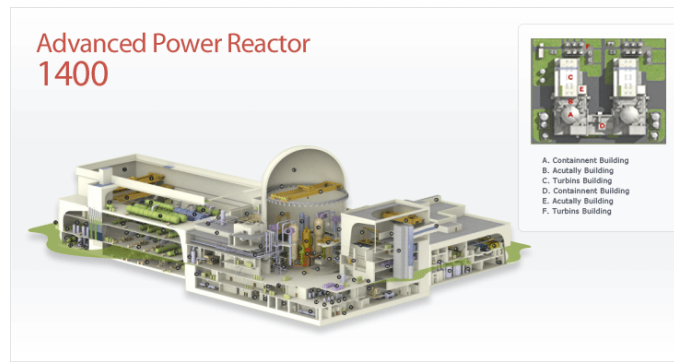
1994~2008



2008~

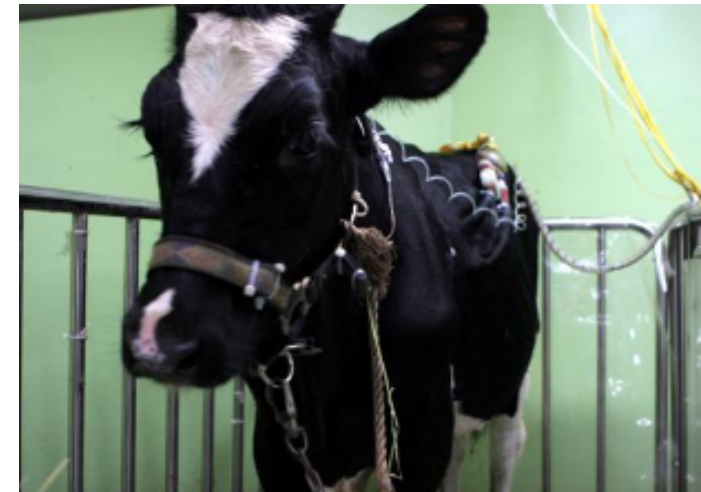


UCI, 1981



KNICS (Korea Nuclear I&C System)

Reactor Protection Software



Artificial Heart (HVAD)



MIT, 2013

- **Software qualification for digital safety system (2001~2007)**

focus 1
embedded software.....

Formal Modeling and Verification of Safety-Critical Software

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Eunyoung Jee, Korea Advanced Institute of Science and Technology

Sungdeok Cha, Korea University

A formal-methods-based process for developing safety-critical software supports development, verification and validation, and safety analysis and has proven to be effective and easy to apply.

Rigorous quality demonstration is important when developing safety-critical software such as a nuclear power plant's reactor protection system (RPS). Although stakeholders strongly recommend using formal modeling and verification, domain experts often reject such methods because the candidate techniques are overabundant, the notations appear complex, the tools often work only in isolation, and the output is frequently too difficult for domain experts to understand and to extract meaningful information.

To overcome such obstacles, we developed a formal-methods-based process that supports development, verification, and safety analysis. We also developed CASE tools to let nuclear engineers apply formal methods without having to know the underlying formalism in depth. In this article, we describe more than seven years' experience working with nuclear engineers in developing RPS software and applying formal methods. Nuclear engineers and regulatory personnel found the process effective and easy to apply with our integrated tool

a digital control system for the APR-1400 reactor. At the project's start, project managers made two decisions that strongly influenced our process:

- When developing safety-critical components such as an RPS, we would use formal methods whenever it was practical to do so.
- Software development would be based on the programmable logic controller (PLC), using function block diagram (FBD) as the implementation language.



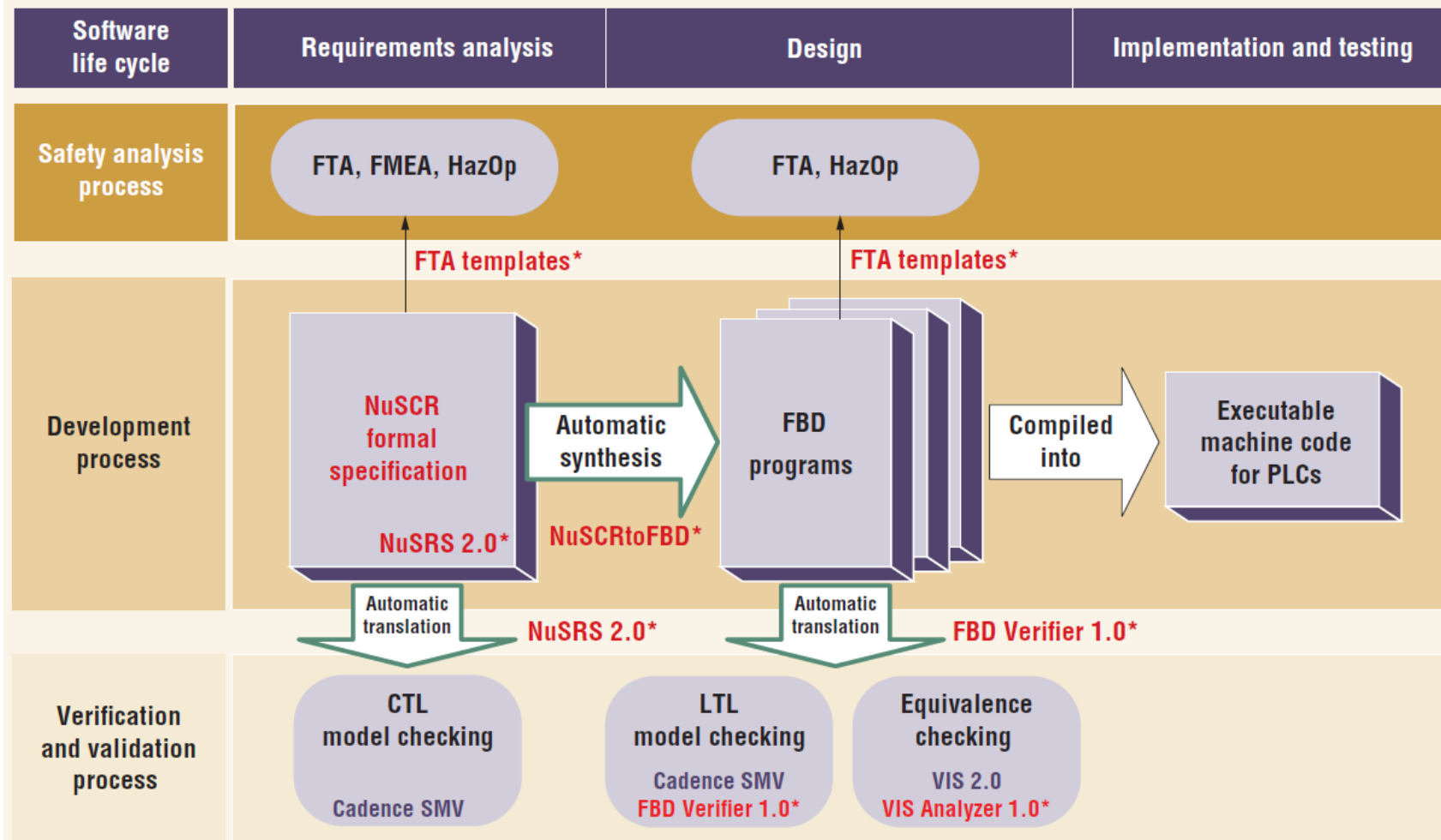
IEEE Software,
May/June 2009

More on KNICS Project

- **Programmable Logic Controller(PLC)-based software development**
 - Using function block diagram (FBD) as the implementation language
 - “Project environment” to our group
- **Formal methods were used whenever practical**
 - To automate as much analysis as possible
 - To reduce human errors
 - To provide greater safety assurance
 - Our group’s own decision



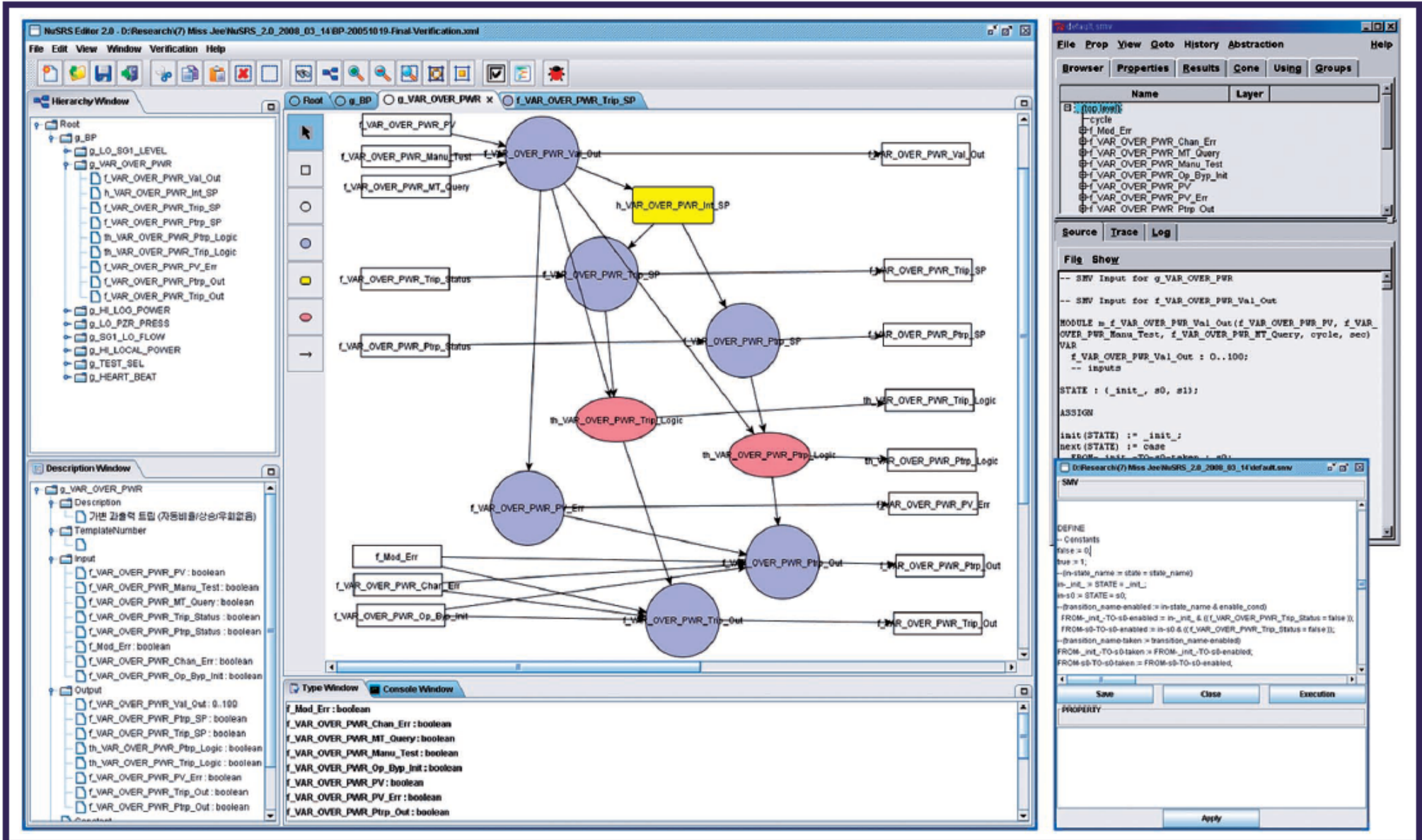
Our Approach



CTL Computation tree logic
 FBD Function block diagram
 FMEA Failure modes and effects analysis
 FTA Fault tree analysis
 HazOp Hazard and operability study
 LTL Linear temporal logic

NuSCR Software cost reduction for nuclear applications
 NuSRS CASE tool for NuSCR specification and verification
 PLC Programmable logic controller
 SMV Symbolic model verifier
 VIS Verification Interacting with Synthesis

Requirements Engineering



The screenshot displays the NuSRS Editor 2.0 interface, showing a state machine diagram for a power over current protection system. The diagram consists of several states (circles) and transitions (arrows) triggered by events (rectangles). A state named `h_VAR_OVER_PWR_Val_SP` is highlighted in yellow.

State Machine Diagram:

- States:**
 - `f_VAR_OVER_PWR_FV` (blue circle)
 - `h_VAR_OVER_PWR_Val_SP` (yellow circle)
 - `f_VAR_OVER_PWR_Trip_SP` (blue circle)
 - `h_VAR_OVER_PWR_Ptp_SP` (blue circle)
 - `h_VAR_OVER_PWR_Trip_Logic` (red circle)
 - `h_VAR_OVER_PWR_Ptp_Logic` (red circle)
 - `f_VAR_OVER_PWR_PV_Err` (blue circle)
 - `h_VAR_OVER_PWR_Trip_Out` (blue circle)
 - `h_VAR_OVER_PWR_Ptp_Out` (blue circle)
- Transitions:**
 - `f_VAR_OVER_PWR_Manu_Test` and `f_VAR_OVER_PWR_Mt_Query` trigger transitions to `f_VAR_OVER_PWR_FV`.
 - `f_VAR_OVER_PWR_Trip_Status` and `f_VAR_OVER_PWR_Ptp_Status` trigger transitions to `f_VAR_OVER_PWR_Trip_SP` and `f_VAR_OVER_PWR_Ptp_SP` respectively.
 - `h_VAR_OVER_PWR_Val_SP` triggers transitions to `h_VAR_OVER_PWR_Trip_Logic` and `h_VAR_OVER_PWR_Ptp_Logic`.
 - `h_VAR_OVER_PWR_Trip_Logic` and `h_VAR_OVER_PWR_Ptp_Logic` trigger transitions to `h_VAR_OVER_PWR_Trip_Out` and `h_VAR_OVER_PWR_Ptp_Out` respectively.
 - `f_Mod_Err`, `f_VAR_OVER_PWR_Chan_Err`, `f_VAR_OVER_PWR_Mt_Query`, `f_VAR_OVER_PWR_Manu_Test`, `f_VAR_OVER_PWR_Op_Byp_Init`, and `f_VAR_OVER_PWR_PV_Err` trigger transitions to `h_VAR_OVER_PWR_Trip_Out` and `h_VAR_OVER_PWR_Ptp_Out`.

Left Panel (Hierarchy/Description Windows):

- Hierarchy Window:** Shows a tree structure of the project, including `g_BP`, `g_LO_SG1_LEVEL`, `g_VAR_OVER_PWR`, and various sub-states like `h_VAR_OVER_PWR_Val_Out`, `h_VAR_OVER_PWR_Int_SP`, `h_VAR_OVER_PWR_Trip_SP`, `h_VAR_OVER_PWR_Ptp_SP`, `h_VAR_OVER_PWR_Trip_Logic`, `h_VAR_OVER_PWR_Ptp_Logic`, `f_VAR_OVER_PWR_PV_Err`, `f_VAR_OVER_PWR_Ptp_Out`, `f_VAR_OVER_PWR_Trip_Out`, `g_H_LOG_POWER`, `g_LO_PZR_PRESS`, `g_SG1_LO_FLOW`, `g_H_LOCAL_POWER`, `g_TEST_SEL`, and `g_HEART_BEAT`.
- Description Window:** Shows the description for `g_VAR_OVER_PWR`, including a description in Korean, a template number, and a list of input and output signals with their data types (e.g., `boolean`, `0..100`).

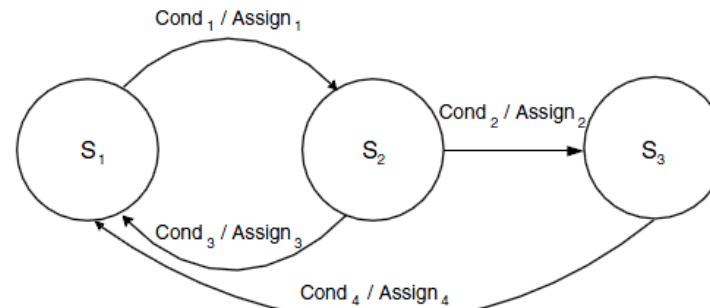
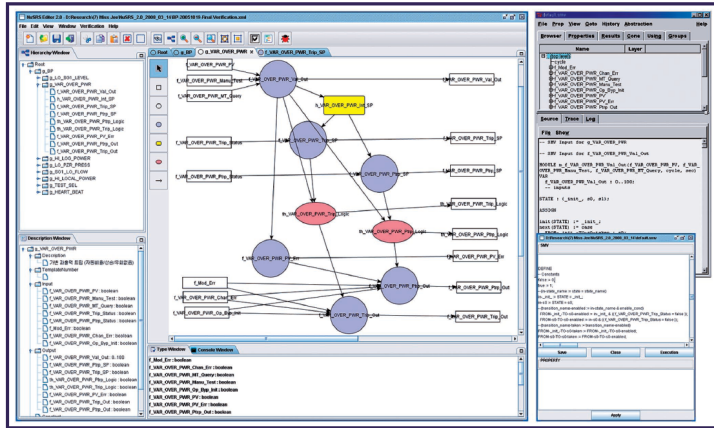
Right Panel (File Show):

Shows the source code for the state machine, including the module definition and the state machine logic.

```

-- SHV Input for g_VAR_OVER_PWR
-- SHV Input for f_VAR_OVER_PWR_Val_Out
MODULE h f_VAR_OVER_PWR_Val_Out (f_VAR_OVER_PWR_PV, f_VAR_OVER_PWR_Manu_Test, f_VAR_OVER_PWR_Mt_Query, cycle, sec)
VAR
  f_VAR_OVER_PWR_Val_Out : 0..100;
  -- inputs
STATE : (_init_, s0, s1);
ASSIGN
  init (STATE) := _init_;
  next (STATE) := case
    FROM _init_ TO s0 taken := s0;
  DEFINE
  -- Constants
  false = 0;
  true = 1;
  --(in-state_name = s0 => state_name)
  in_init_ := STATE = _init_;
  in_s0 := STATE = s0;
  --(transition_name-enabled := in-state_name & enable_cond)
  FROM_in_s0-to-s0-enabled := in_init_ & ((f_VAR_OVER_PWR_Trip_Status = false));
  FROM_s0-to-s0-enabled := in_s0 & ((f_VAR_OVER_PWR_Trip_Status = false));
  --(transition_name-taken = transition_name-enabled)
  FROM_in_s0-to-s0-taken := FROM_in_s0-to-s0-enabled;
  FROM_s0-to-s0-taken := FROM_s0-to-s0-enabled;
  
```

Requirements Modeling



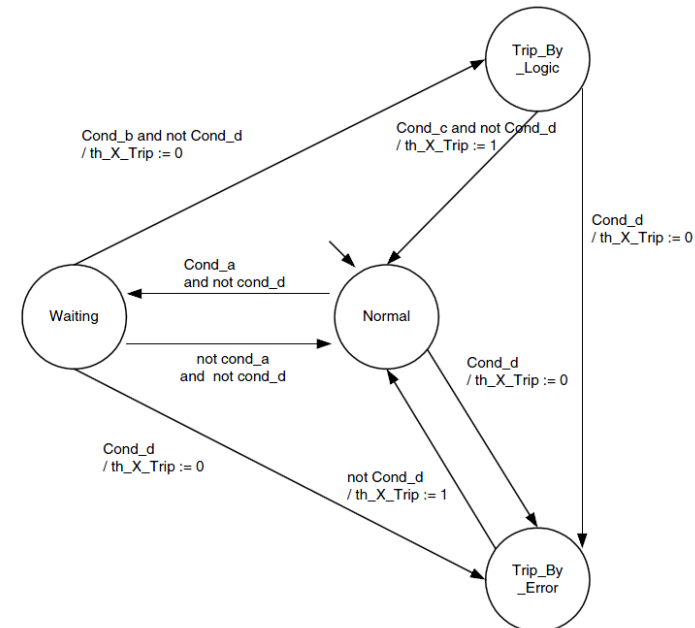
History node

Fig. 7. Finite state machine for history variable node.

Conditions			
Cond ₁	T	-	T
Cond ₂	F	T	-
Cond ₃	-	F	T
Actions			
Assign ₁	X		
Assign ₂		X	
Assign ₃			X

Fig. 6. Structured decision table for a function variable.

Function node



Timed-History node

Cond_a : $f_X \geq k_X_Trip_Setpoint$
 Cond_b : $[k_Trip_Delay, k_Trip_Delay] (f_X \geq k_X_Trip_Setpoint \text{ and } h_X_OB_Sta = 0)$
 Cond_c : $f_X < k_X_Trip_Setpoint - k_X_Trip_Hys$
 Cond_d : $f_X_Valid = 1 \text{ or } f_Module_Error = 1 \text{ or } f_Channel_Error = 1$

Fig. 3. Timed transition system for $th_X.Trip$.

Requirements Modeling

- Attempted to balance between readability, expressiveness, and analyzability
 - Preference of stakeholder, in particular the regulatory body, was taken into consideration
 - Approval experience on Wolsung NPP 2-3-4 shutdown system (1995~1997)

Conditions			
Cond ₁	T	-	T
Cond ₂	F	T	-
Cond ₃	-	F	T
Actions			
Assign ₁	X		
Assign ₂		X	
Assign ₃			X

Fig. 6. Structured decision table for a function variable.

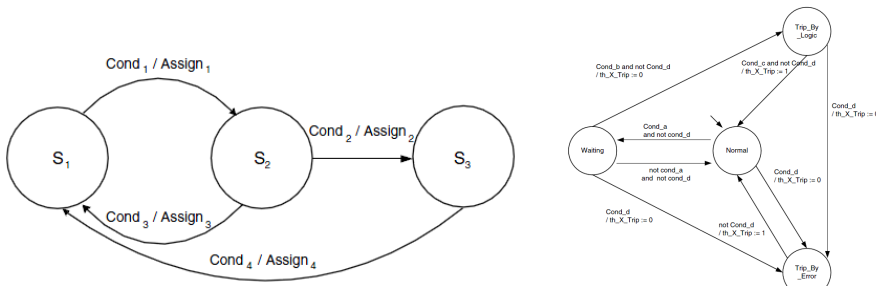
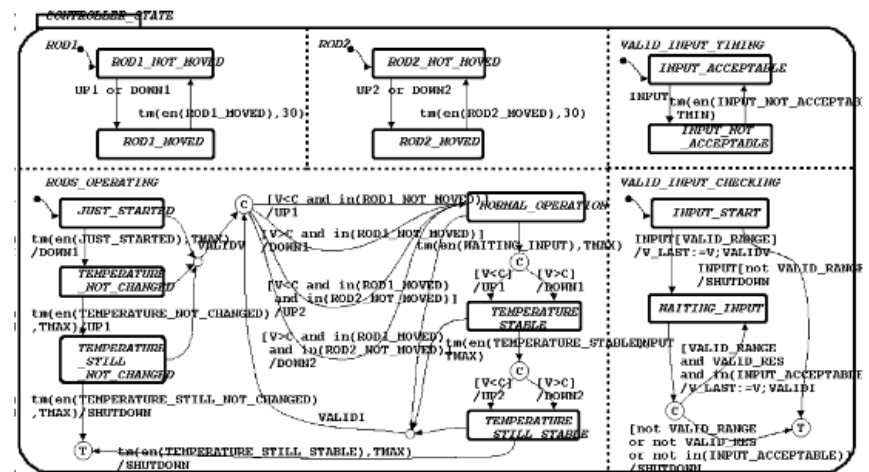


Fig. 7. Finite state machine for history variable node.

VS



Cond a : $f \cdot X \Rightarrow k \cdot X$ Trip_Setpoint
 Cond b : $f \cdot X \Rightarrow k \cdot X$ Trip_Setpoint / if $X \Rightarrow k \cdot X$ Trip_Setpoint and $f \cdot X$ OR $S_{sta} = 0$
 Cond c : $f \cdot X \Rightarrow k \cdot X$ Trip_Setpoint \wedge X Trip_Setpoint
 Cond d : $f \cdot X$ Value = 1 or f Module_Error = 1 or f Channel_Error = 1
 Fig. 3. Timed transition system for $A_{1,2}$ Trip.

Requirements Modeling


- **Defined notations AND formal semantics**
- **Automated much of requirements analysis**
 - Completeness, consistency, ...
 - Model checking



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A formal software requirements specification method for digital nuclear plant protection systems

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Abstract

This article describes NuSCR, a formal software requirements specification method for digital plant protection system in nuclear power plants. NuSCR improves the readability and specifiability by providing graphical or tabular notations depending on the type of operations. NuSCR specifications can be formally analyzed for completeness, consistency, and against the properties specified in temporal logic. We introduce the syntax and semantics of NuSCR and demonstrate the effectiveness of the approach using reactor protection system, digital protection system being developed in Korea, as a case study.

FBD Synthesis

- Was feasible due to relatively small (and intended) semantic gap

Conditions			
Cond ₁	T	-	T
Cond ₂	F	T	-
Cond ₃	-	F	T
Actions			
Assign ₁	X		
Assign ₂		X	
Assign ₃			X

Fig. 6. Structured decision table for a function variable.

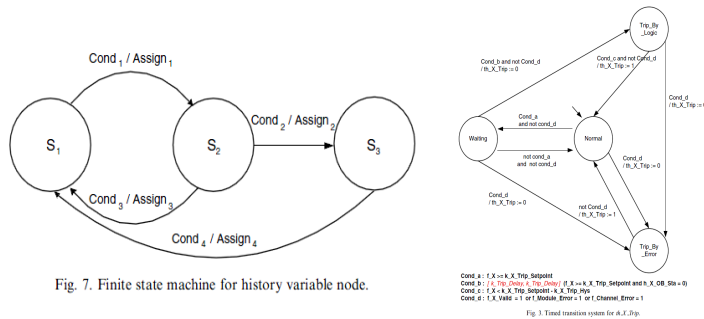
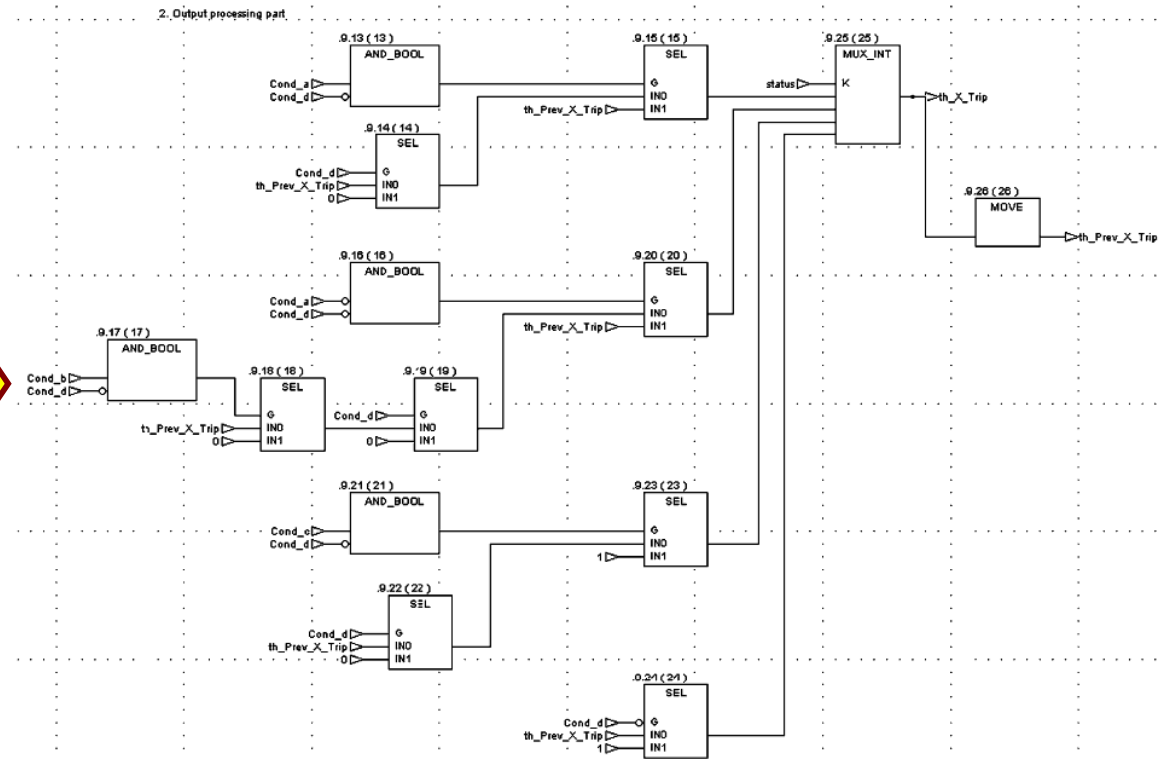


Fig. 7. Finite state machine for history variable node.



Synthesized FBD was NOT Optimized

- state- and history-dependent nodes posed challenge

Table 1
Comparison of the number of FBD blocks included in the fixed set-point rising trip logic

	<i>f_X_Valid</i>	<i>th_X_Trip</i>	<i>th_X_Pretrip</i>	<i>F_X_OB_Perm</i>	<i>h_X_OB_Sta</i>	Total
System atically generated from NuSCR	3	39	16	2	11	71
Manually generated by experts	3	12	8	9		32

Number of function blocks used.

Table 2
Comparison of the number of function blocks used for the representative trip logics in BP

Trip logic for BP	Mechanically generated from NuSCR	Manually generated by experts
Fixed set-point rising trip with operating bypass	71	32
Fixed set-point rising trip without operating bypass	53	24
Auto-limited rate variable set point trip without operating bypass	95	40
Manual reset variable set point trip with operating bypass	117	67
Total	336	163

Number of function blocks used.



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Synthesis of FBD-based PLC design from NuSCR formal specification

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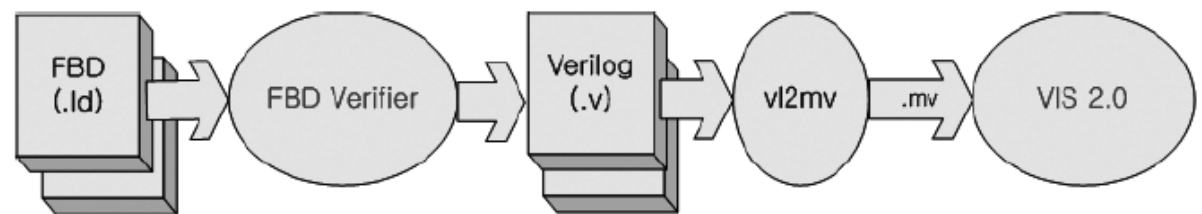
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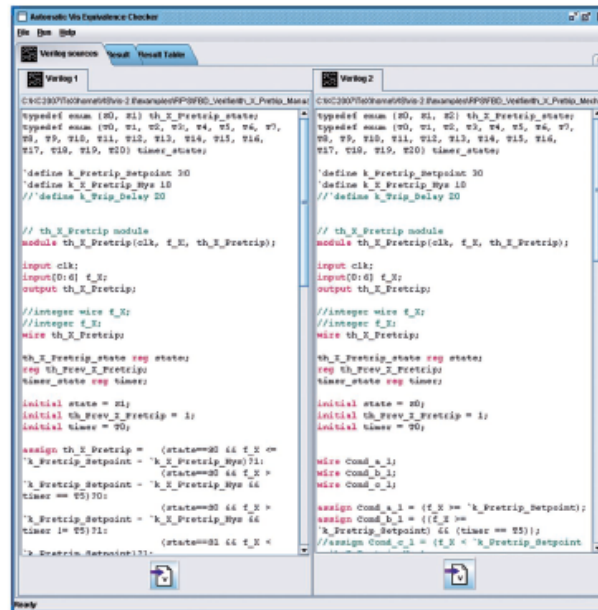
FBD Verification and VIS

- Manual optimization of FBD code was inevitable
- Used VIS (Verification Interacting with Synthesis) to support subsequent behavioral equivalence
 - Defined FBD translation rules into Verilog

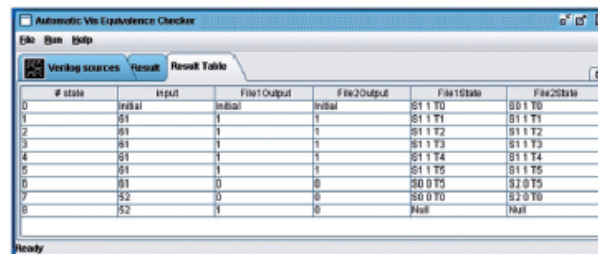


Intuitive and Visual Analysis

- To help domain experts better understand results

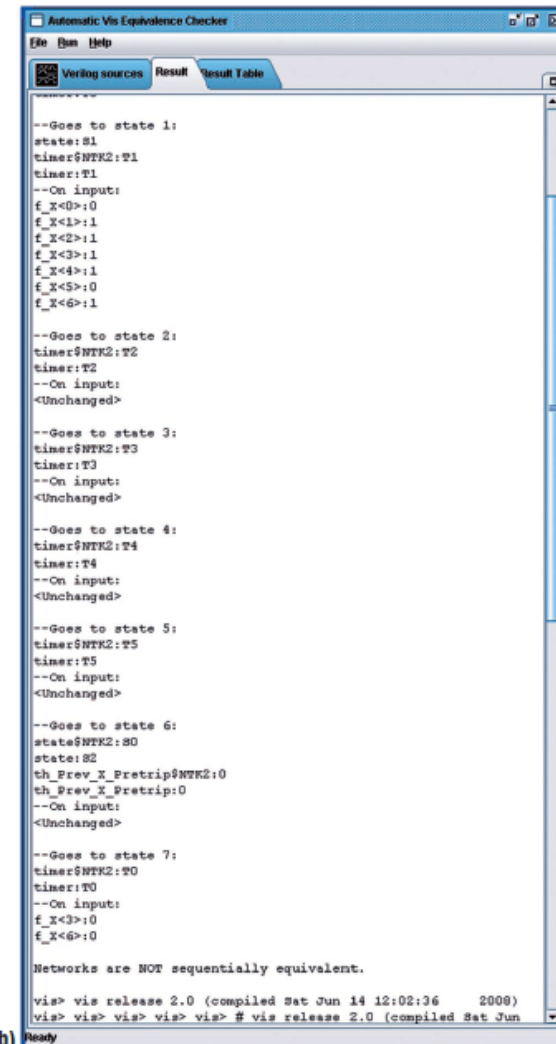


(a)



# state	#in0	input	#in1Output	#in2Output	#in1State	#in2State
0	#in0		#in0		S11 Y0	S11 Y0
1	S1	1	1	1	S11 T1	S11 T1
2	S1	1	1	1	S11 T2	S11 T2
3	S1	1	1	1	S11 T3	S11 T3
4	S1	1	1	1	S11 T4	S11 T4
5	S1	1	1	1	S11 T5	S11 T5
6	S1	0	0	0	S20 T5	S20 T5
7	S2	0	0	0	S20 Y0	S20 Y0
8	S2	1	0	Null	Null	Null

(c)



```

--Goes to state 1:
state:S1
timer$NTK2:T1
timer:T1
--On input:
f_X<0>:0
f_X<1>:1
f_X<2>:1
f_X<3>:1
f_X<4>:1
f_X<5>:0
f_X<6>:1

--Goes to state 2:
timer$NTK2:T2
timer:T2
--On input:
<Unchanged>

--Goes to state 3:
timer$NTK2:T3
timer:T3
--On input:
<Unchanged>

--Goes to state 4:
timer$NTK2:T4
timer:T4
--On input:
<Unchanged>

--Goes to state 5:
timer$NTK2:T5
timer:T5
--On input:
<Unchanged>

--Goes to state 6:
state$NTK2:S0
state:S2
th_Prev_X_Pretrip$NTK2:0
th_Prev_X_Pretrip:0
--On input:
<Unchanged>

--Goes to state 7:
timer$NTK2:T0
timer:T0
--On input:
f_X<3>:0
f_X<6>:0

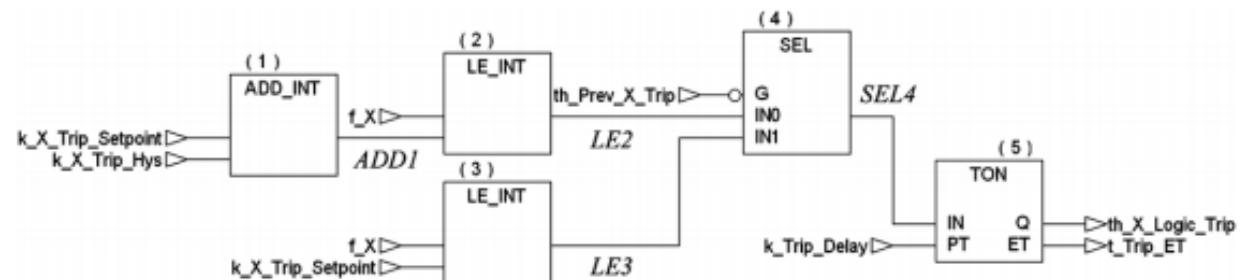
Networks are NOT sequentially equivalent.

vis> vis release 2.0 (compiled Sat Jun 14 12:02:36 2008)
vis> vis> vis> vis> vis> # vis release 2.0 (compiled Sat Jun
  
```

(b)

- **FBD, based on its data-flow model, posed particular challenge**
 - Any test case would satisfy 100% coverage with simplistic definition
- **Had to define a customized coverage criteria to satisfy regulatory requirements**

...The two aspects of test coverage that are particularly important for the unit testing of safety system software are *coverage of requirements* and *coverage of the internal structure of the code*.
 ... For safety system software, the unit test coverage criteria to be employed should be identified and justified. ... [USNRC Regulation Guide 1.171] [4]

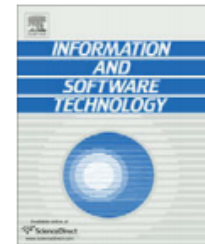




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A data flow-based structural testing technique for FBD programs

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ABSTRACT

With increased use of programmable logic controllers (PLCs), software assurance became an important issue. Real-time control systems by identifying coverage criteria, based on control flow graph and function block diagram (FBD) which is a three structural coverage criteria for FBD. We tested their effectiveness using a real-world example prepared by FBD testing professionals, and the results were tested sufficiently. Domain experts, however, have been effective.



FBD-customized coverage criteria

- **Defined conditions under which specific input played direct role in determining the output**
 - d-path condition
- **Defined various coverage criteria under which various FBD unit testing could be performed**
 - Basic coverage, input condition coverage, complex condition coverage
 - Similar to statement coverage, branch coverage, condition coverage in traditional (procedural) software testing

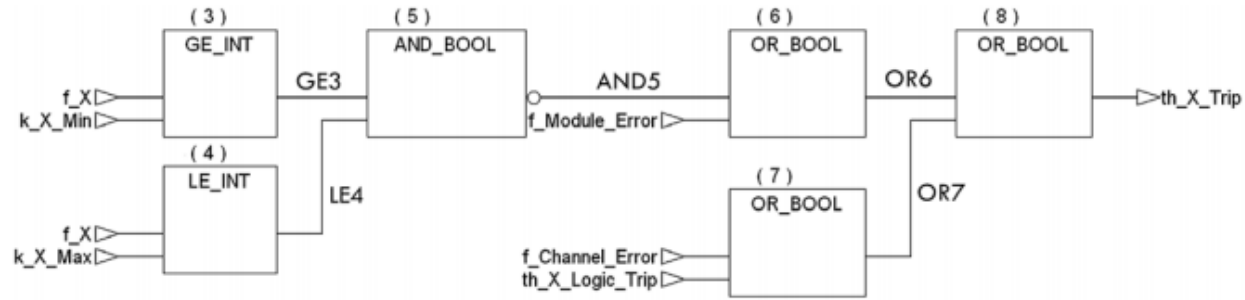


Fig. 5. A simplified FBD program for calculating th_X_Trip .

(a) Coverage Result for **Basic Coverage Criterion**

Test Set	Test Requirements							#Test Reqs (Satisfied/Total)	Coverage (%)
	DPC(p ₃₁)	DPC(p ₃₂)	DPC(p ₃₃)	DPC(p ₅₁)	DPC(p ₅₂)	DPC(p ₅₃)	DPC(p ₅₄)		
TS1	O	O	O	O	O	O	O	7/7	100%

(b) Coverage Result for **Input Condition Coverage Criterion**

Test Set	Test Requirements										#Test Reqs (Satisfied/Total)	Coverage (%)
	DPC(p ₃₁) ^ ME	DPC(p ₃₁) ^ ¬ME	DPC(p ₃₂) ^ CE	DPC(p ₃₂) ^ ¬CE	DPC(p ₃₃) ^ LT	DPC(p ₃₃) ^ ¬LT	DPC(p ₅₁)	DPC(p ₅₂)	DPC(p ₅₃)	DPC(p ₅₄)		
TS1	X	O	X	O	X	O	O	O	O	O	7/10	70%
TS2	O	O	O	O	O	O	O	O	O	O	10/10	100%

(c) Coverage Result for **Complex Condition Coverage Criterion**

Test Set	Test Requirements						#Test Reqs (Satisfied/Total)	Coverage (%)
	DPC(p ₃₁) ^ ME	DPC(p ₃₁) ^ ¬ME	DPC(p ₃₁) ^ OR6	DPC(p ₃₁) ^ ¬OR6	DPC(p ₃₁) ^ TR	DPC(p ₃₁) ^ ¬TR		
TS1	X	O	X	O	X	O	...	
TS2	O	O	O	O	O	O		
TS3	O	O	O	O	O	O		

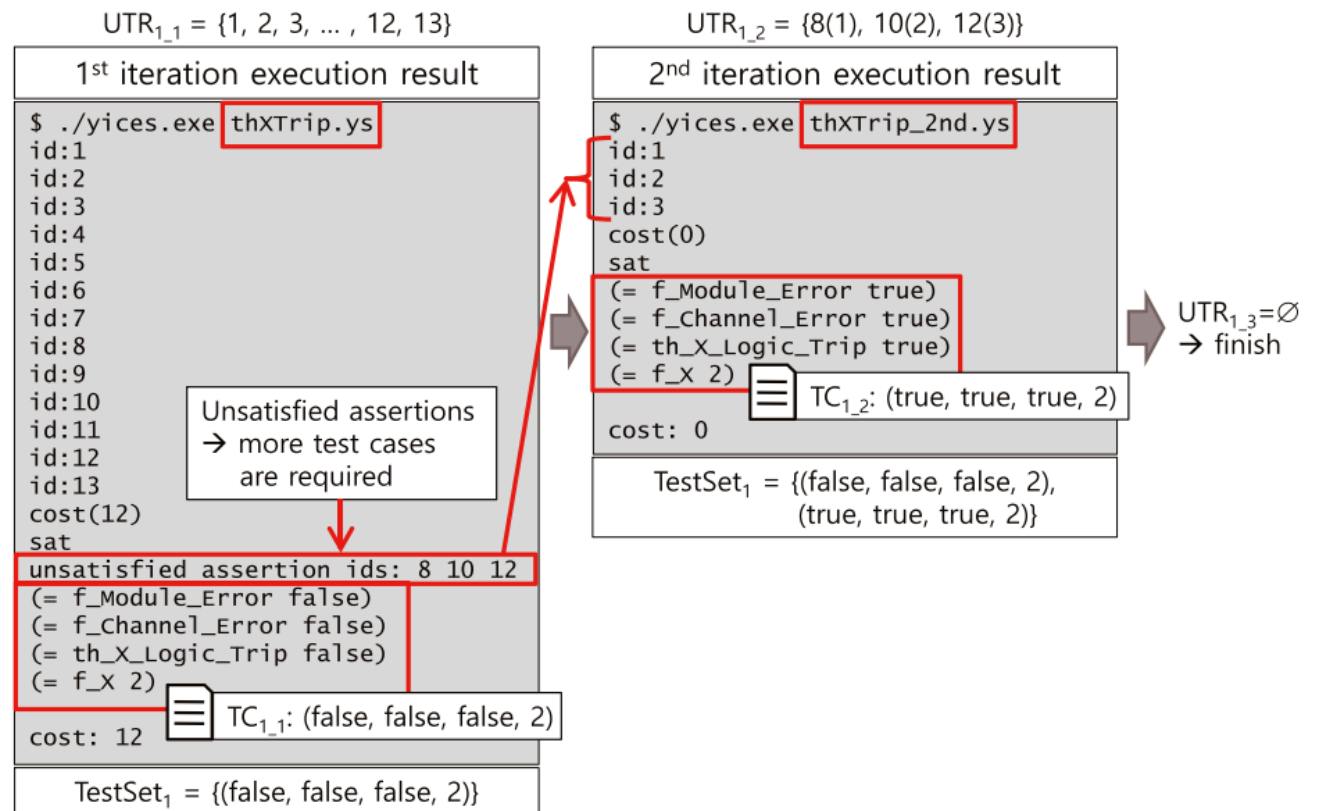
	Test Requirements								#Test Reqs (Satisfied/Total)	Coverage (%)
	DPC(p ₅₄) ^ LE4	DPC(p ₅₄) ^ ¬LE4	DPC(p ₅₄) ^ AND5	DPC(p ₅₄) ^ ¬AND5	DPC(p ₅₄) ^ OR6	DPC(p ₅₄) ^ ¬OR6	DPC(p ₅₄) ^ TR	DPC(p ₅₄) ^ ¬TR		
	O	X	X	O	X	O	X	O	25/50	50%
	O	X	X	O	X	O	X	O	34/50	68%
	O	O	O	O	O	O	O	O	50/50	100%

For the input vector (f_X, f_Module_Error, f_Channel_Error, f_X_Logic_Trip),
 TS1 = { (2, 0, 0, 0) }
 TS2 = { (2, 0, 0, 0), (2, 1, 1, 1) }
 TS3 = { (2, 0, 0, 0), (2, 1, 1, 1), (0, 0, 1, 1), (99, 0, 1, 1) }

ME: f_Module_Error
 CE: f_Channel_Error
 LT: th_X_Logic_Trip
 TR: th_X_Trip

Fig. 6. Coverage assessment result for the FBD program in Fig. 5.

- **Developed a tool to automate test case generation (Jee et al., STVR, 2014)**
 - Used Yices, an SMT solver developed by SRI International

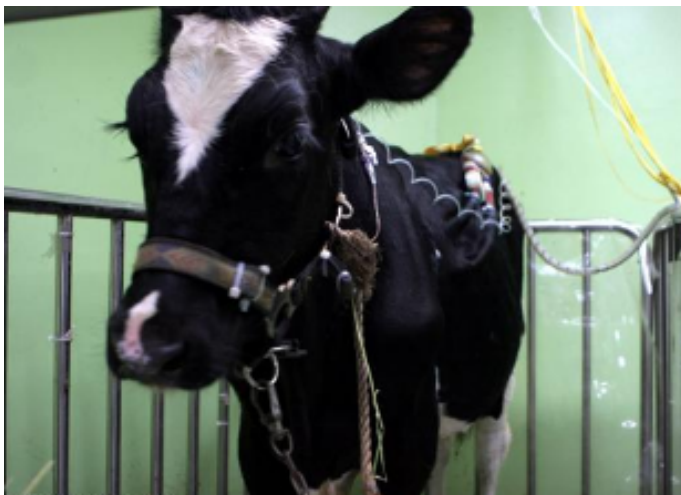
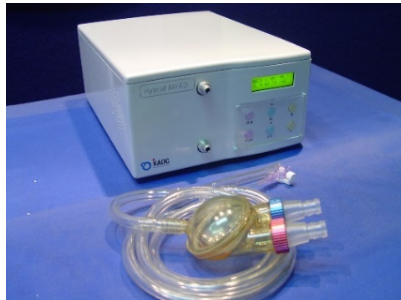


KNICS Lessons

- **Be flexible and attentive to stakeholders' needs**
 - Including regulatory personnel when relevant
- **“Let them do the work” ;)**
 - Extremely important that SE professionals communicate and work well with domain experts
 - It is NEVER as easy as it seems
- **Do not reinvent wheels. SMV, VIS, Yices, ...**
- **Provide data visualization/interpretation tools**
- **Domain-specific problems can become interesting SE challenges (e.g., FBD testing criteria)**

Hybrid Ventricular Assist Device

- Korea Artificial Organ Center (KAOC) project
- Animal-tested for 183 days on a calf, exceeding the FDA regulations on long-term experiment
 - No anomaly was detected



뉴스홈 > 의료

등록날짜 2007년 08월 13일 00시 00분

기사 크기

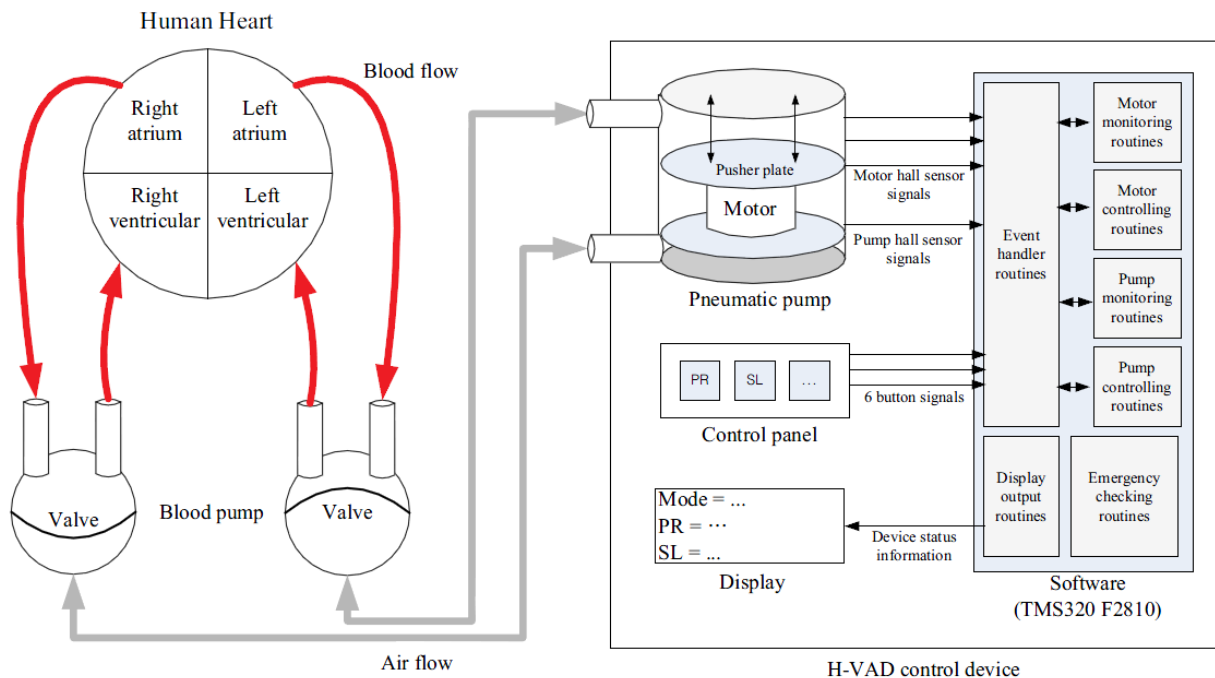
국산 인공심장 이식 송아지, 국내 최장 70일 생존
 高大 한국인공장기센터 연구팀, 인공장기상용화 전기마련



고려대 한국인공장기센터(소장 선경, 안암병원 흉부외과)가 인공심장을 이식한 송아지가 국내 최장 생존 기록 70일을 세워, 의학계의 관심이 쏠리고 있다. 종전 45일보다 25일 이상 오래 생존한 기록이다.

이번에 이식한 인공심장 H-VAD는 고려대 한국인공장기센터가 자체 개발한 것이다. 이로써 국내기술로 만든 인공심장으로서는 최장 생존기록을 달성했다는 점이 의미가 깊다.

- **Event-driven architecture**
 - Pumping Rate (PR), Stroke Length (SL), Start / Stop button
 - 211 probing statements were added
- **Control logic in ~3,800 LoC in C**
 - Relatively simple branch conditions



```
switch(CMKBIT(Control_Flag, BIT01)) {
case B1SET : // Brake-time Process
/*****/
visited(1, 1, 11);
/*****/
if(CMKBIT(Control_Flag, BIT02) == B2SET) { // if left_end_position,
/*****/
visited(1, 1, 12);
/*****/
if( Ref Left Brake Time < Real Left Brake Time ) {
/*****/
visited(1, 1, 13);
/*****/
if( Op_Status != EMERGENCY_OP_2 ) { // if abnormal stop not occurred,
/*****/
visited(1, 1, 14);
/*****/
// PR_Calculation
// 0.001 * PR_Counter (sec) : 1 = 60 (sec) : Pump_Rate
```

Time Interrupt Function

In-Vitro Testing

- Each button was pressed at least once
- All permitted parameter values were covered (e.g., SL 30~90, default 60)
- Stop button was pressed at arbitrary and random moments



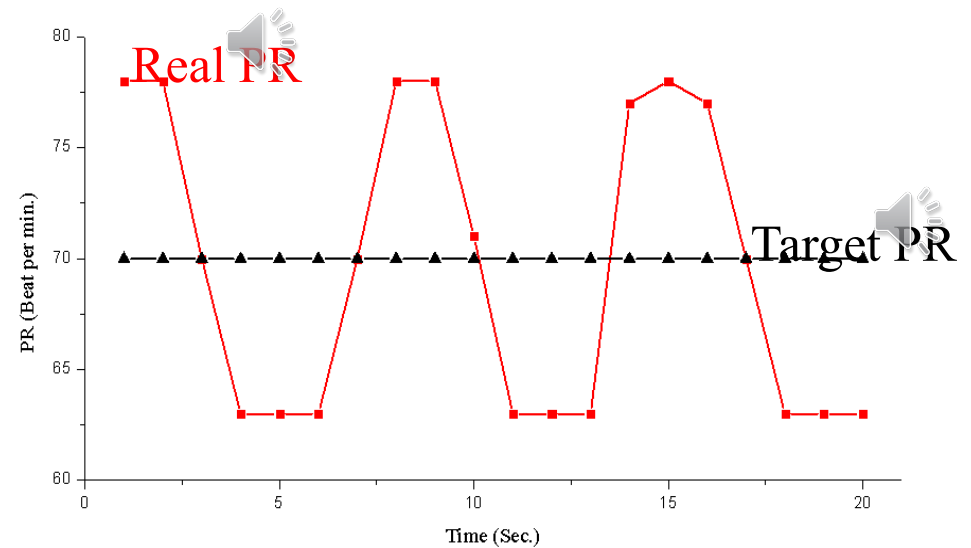
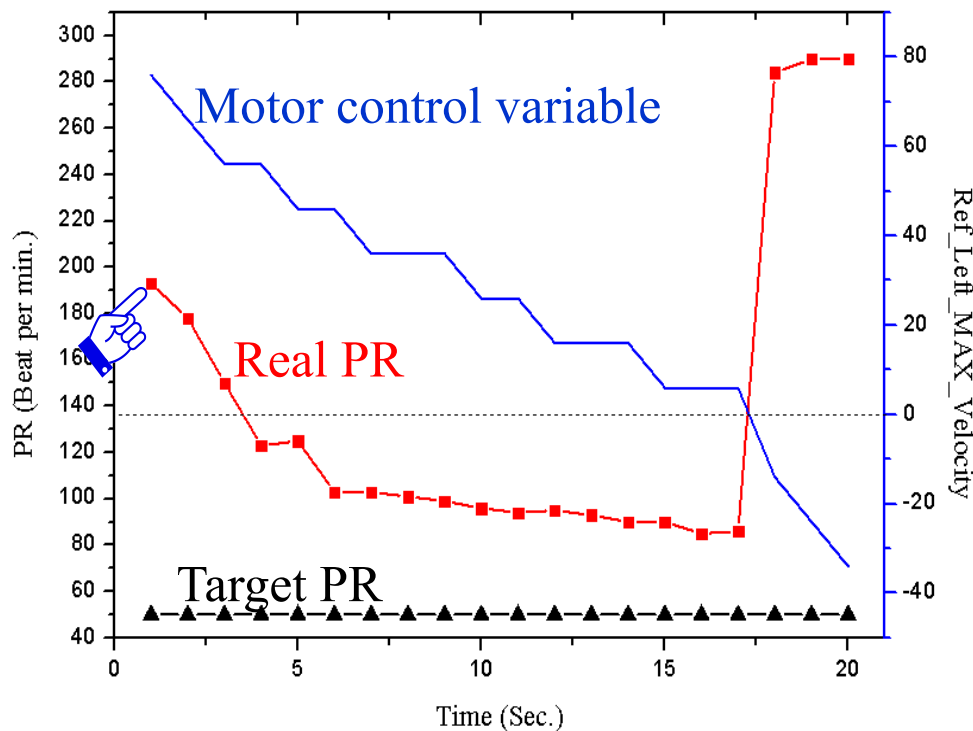
In-Vitro Testing

- Tried to force the system to engage in predefined emergency modes
- Achieved 80.6%, 170 out of 211 probes, coverage

ID	Test inputs	Precondition						Related Guide line	Description
		PR	SL	Control mode	Running mode	Pump position	Pump direction		
TC1	START	50	60	PR	STOP	Center	N/A	1	Baseline
TC2	Plus (10 times)	50	60	PR	RUNNING	N/A	N/A	2	Increasing pump rate
TC3	Plus	150	60	PR	RUNNING	N/A	N/A	3	Upper boundary checking for pump rate
TC4	Minus (10 times)	50	60	PR	RUNNING	N/A	N/A	2	Decreasing pump rate
TC5	Minus	5	60	PR	RUNNING	N/A	N/A	3	Lower boundary checking for pump rate
TC6	SL	50	60	PR	RUNNING	N/A	N/A	1	Changing the control mode
TC7	Plus (10 times)	50	60	SL	RUNNING	N/A	N/A	2	Increasing stroke length
TC8	Plus	50	80	SL	RUNNING	N/A	N/A	3	Upper boundary checking for stroke length
TC9	Minus (10 times)	50	60	SL	RUNNING	N/A	N/A	2	Decreasing stroke length
TC10	Minus	50	30	SL	RUNNING	N/A	N/A	3	Lower boundary checking for stroke length
TC11	PR	50	60	SL	RUNNING	N/A	N/A	1	Changing the control mode
TC12	Plus (10 times)	50	60	PR	STOP	N/A	N/A	2	Same with TC2 but in stopped mode
TC13	Plus	150	60	PR	STOP	N/A	N/A	3	Same with TC3 but in stopped mode
TC14	Minus (10 times)	50	60	PR	STOP	N/A	N/A	2	Same with TC4 but in stopped mode
TC15	Minus	5	60	PR	STOP	N/A	N/A	3	Same with TC5 but in stopped mode
TC16	SL	50	60	PR	STOP	N/A	N/A	1	Same with TC6 but in stopped mode
TC17	Plus (10 times)	50	60	SL	STOP	N/A	N/A	2	Same with TC7 but in stopped mode
TC18	Plus	50	80	SL	STOP	N/A	N/A	3	Same with TC8 but in stopped mode
TC19	Minus (10 times)	50	60	SL	STOP	N/A	N/A	2	Same with TC9 but in stopped mode
TC20	Minus	50	30	SL	STOP	N/A	N/A	3	Same with TC10 but in stopped mode
TC21	PR	50	60	SL	STOP	N/A	N/A	1	Same with TC11 but in stopped mode
TC22	STOP	N/A	N/A	N/A	RUNNING	Top	Up	4	Pressing STOP button when the pump is going up from the center position
TC23	STOP	N/A	N/A	N/A	RUNNING	Center	Up	4	Pressing STOP button when the pump is passing the center position and the direction is up.
TC24	STOP	N/A	N/A	N/A	RUNNING	Bottom	Up	4	Pressing STOP button when the pump is going up from the bottom
TC25	STOP	N/A	N/A	N/A	RUNNING	Top	Down	4	Pressing STOP button when the pump is going down from the top
TC26	STOP	N/A	N/A	N/A	RUNNING	Center	Down	4	Pressing STOP button when the pump is passing the center position and the direction is down.
TC27	STOP	N/A	N/A	N/A	RUNNING	Bottom	Down	4	Pressing STOP button when the pump is going down from the center position
TC28	Disable center hall sensor	N/A	N/A	N/A	RUNNING	N/A	N/A	5	Triggering emergency mode 1
TC29	Block air valve	N/A	N/A	N/A	RUNNING	N/A	N/A	5	Triggering emergency mode 2

In-Vitro Testing: Results

- Found two behavior patterns, previously unknown to KAOC staff, that appeared abnormal



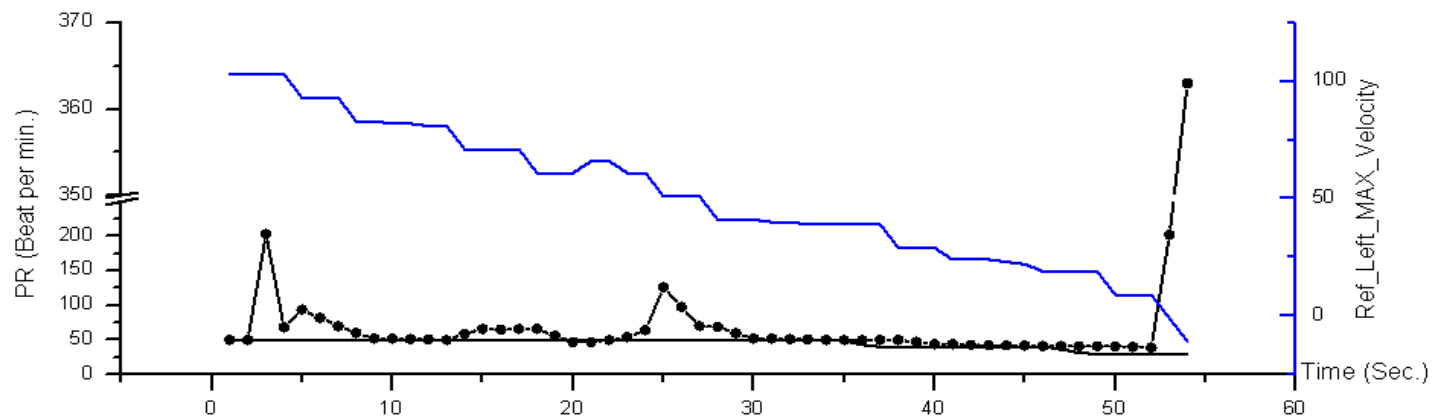
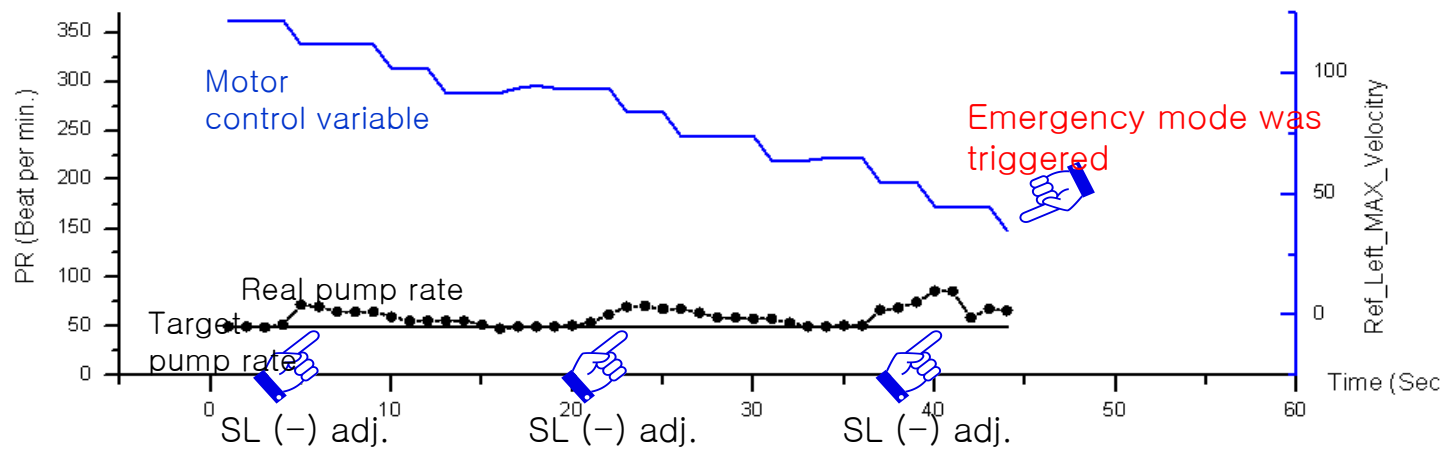
Animal Testing and H-VAD Software

- **Used two 3-months old piglets**
- **78.7% code coverage (cf 80.6%)**
 - Due to our inability to force/repeat certain test cases without endangering the test animal's life



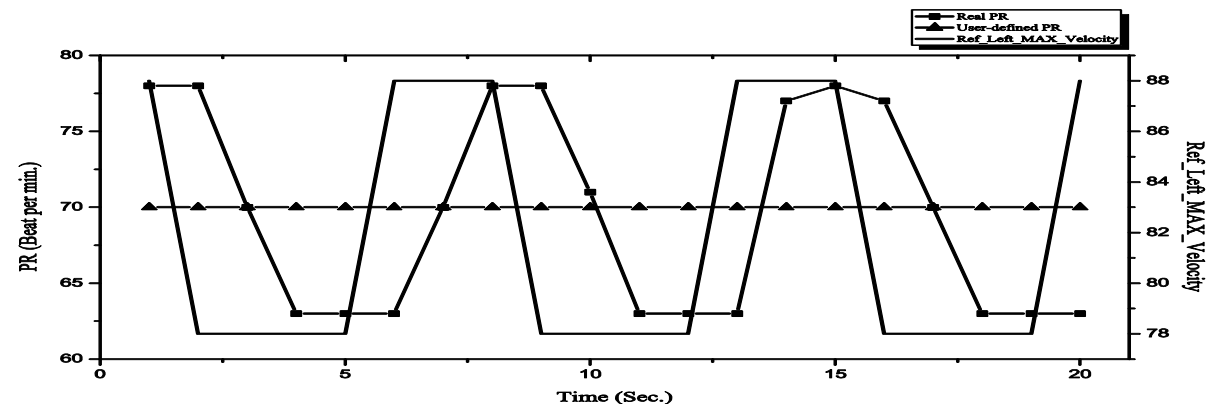
Animal Testing: Results

- **Could NOT recreate in-vitro testing result**

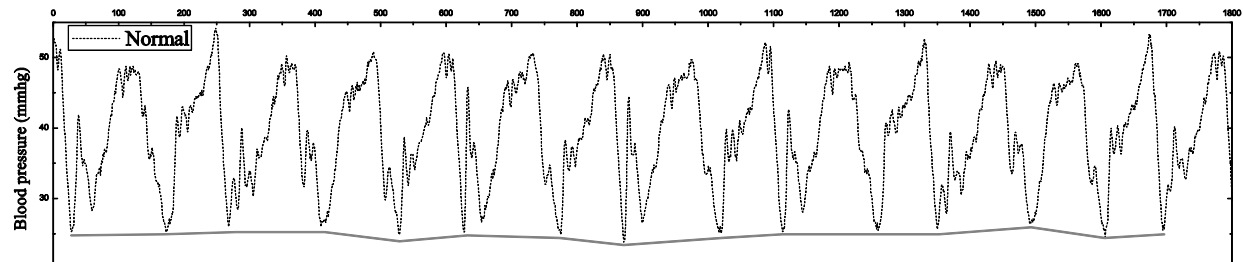


Animal Testing: Results

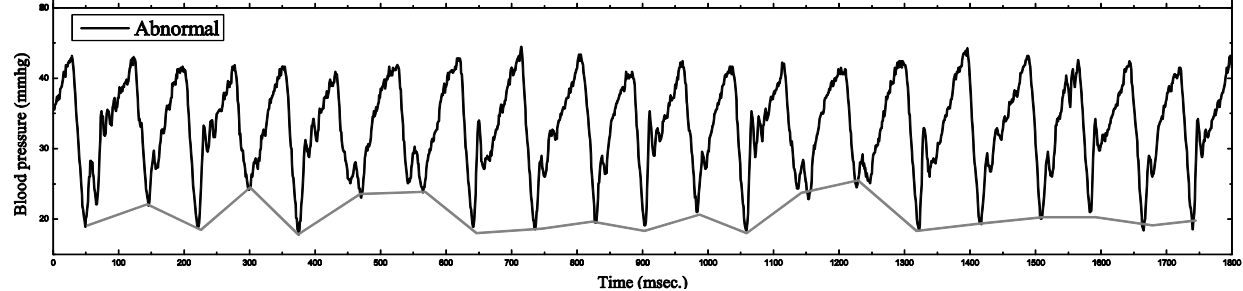
- Abnormal pumping pattern, off by 7, repeated



Normal



Abnormal



H-VAD Lessons

- **SE techniques, although common sense and trivial to us, are not always applied in practice**
- **“Live” testing is expensive, difficult, time-consuming, ...**
 - It is extremely difficult to make credible claims on software quality in safety-critical setting
- **“All NEW H-VAD” project could not be launched**
 - Guide hardware design so as to simplify software design and enhance software safety assurance
- **Dedicated and continuous involvement of domain experts are crucial to the success**

- **Safety-Critical Systems Symposium, Feb 2011, Southampton, UK**

Testing of Safety-Critical Software Embedded in an Artificial Heart

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Abstract Software is being used more frequently to control medical devices such as artificial heart or robotic surgery system. While much of software safety issues in such systems are similar to other safety-critical systems (e.g., nuclear power plants), domain-specific properties may warrant development of customized techniques to demonstrate fitness of the system on patients. In this paper, we report results of a preliminary analysis done on software controlling a Hybrid Ventricular Assist Device (H-VAD) developed by Korea Artificial Organ Centre (KAOC). It is a state-of-the-art artificial heart which completed animal testing phase. We performed software testing in in-vitro experiments and animal experiments. An abnormal behaviour, never detected during extensive in-vitro analysis and animal testing, was found.

Conclusions

- **Interdisciplinary research is important and do-able, but difficult**
- **Software engineering can and should play important roles in software-driven and software-intensive society**
- **Support domain experts to do their work well**
 - We must learn to work with domain experts